1. (Currently Amended) A method of forming trench isolations comprising the steps of:

providing a semiconductor substrate having a cell array region and a peripheral region;

forming at least one cell trench in the cell array region and at least one peripheral trench wider than the cell trench in the peripheral region of the substrate, wherein the cell and the peripheral trenches have sidewalls;

forming a first dielectric layer that partially fills the cell trench and the peripheral trench over the substrate;

forming at least one photoresist pattern that exposes at least the cell trench partially filled with the first dielectric layer over the substrate;

etching the first dielectric layer formed on the sidewalls of the exposed cell trench using the photoresist pattern as a etch mask;

removing the photoresist pattern;

forming a second capping layer over the substrate where the photoresist pattern is removed before forming a second dielectric layer; and

forming ~~a~~ the second dielectric layer filling the cell trench and the peripheral trench over the substrate where the photoresist pattern is removed.

2. (Original) The method of forming trench isolations according to claim 1, further comprising:

forming a gate dielectric layer over the substrate;

forming a polish stop layer over the gate dielectric layer; and

forming hard mask patterns by patterning the polish stop layer and the gate dielectric layer in turn, wherein the gate dielectric, the polish stop layer, and the hard mask patterns are formed before forming the cell trench and the peripheral trench, and wherein forming the cell trench and peripheral trench is performed using the hard mask patterns as a mask.

3. (Original) The method of forming trench isolations according to claim 2, wherein the gate dielectric layer is formed having a different thickness over the cell array region than over the peripheral region.

4. (Original) The method of forming trench isolations according to claim 3, wherein the thickness of the gate dielectric layer formed over the peripheral region is greater than the thickness of the gate dielectric layer formed over the cell array region.

5. (Original) The method of forming trench isolations according to claim 2, further comprising:

forming an oxide layer over the polish stop layer before forming the hard mask patterns, wherein forming the hard mask patterns is done by patterning the oxide layer, the polish stop layer, and the gate dielectric layer one after another.

6. (Original) The method of forming trench isolations according to claim 1, further comprising:

forming a first capping layer covering at least the sidewalls of the cell trench and the peripheral trench before forming the first dielectric layer.

7. (Original) The method of forming trench isolations according to claim 6, wherein the first capping layer is a MTO or a HTO.

8. (Original) The method of forming trench isolations according to claim 1, wherein the first dielectric layer is a HDP-CVD oxide.

9. (Original) The method of forming trench isolations according to claim 1, wherein etching the first dielectric layer formed on the sidewalls of the cell trench is performed using a wet etching process.

10. (Canceled)

11. (Currently Amended) The method of forming trench isolations according to claim 1 ~~10~~, wherein the second capping layer is a MTO or a HTO.

12. (Original) The method of forming trench isolations according to claim 1, wherein the second dielectric layer is a HDP-CVD oxide or an USG oxide.

13. (Original) A method of forming trench isolations for a non-volatile memory device, comprising the steps of:

providing a semiconductor substrate having a cell array region and a peripheral region;

forming a gate dielectric layer, a polysilicon layer, a polish stop layer one after another over the substrate;

forming hard mask patterns by patterning the polish stop layer, the polysilicon layer, and the gate dielectric layer one after another to expose the substrate, wherein the exposed substrate of the peripheral region is wider than the exposed substrate of the cell array region;

forming at least one cell trench in the cell array region and at least one peripheral trench wider than the cell trench in the peripheral region by etching the exposed substrate, wherein the cell trench and the peripheral trench have sidewalls;

forming a first dielectric layer that partially fills the cell trench and the peripheral trench over the substrate;

forming at least one photoresist pattern that exposes at least the cell trench partially filled with the first dielectric layer over the substrate;

etching the first dielectric layer formed on the sidewalls of the exposed cell trench using the photoresist pattern as a etch mask;

removing the photoresist pattern; and

forming a second dielectric layer filling the cell trench and the peripheral trench over the substrate where the photoresist pattern is removed.

14. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, wherein the gate dielectric layer over the peripheral region is thicker than the gate dielectric layer over the cell array region.

15. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, further comprises forming an oxide layer on the polish stop layer before forming the hard mask patterns, wherein the hard mask patterns are formed by patterning the oxide layer, the polish stop layer, the polysilicon layer, and the gate dielectric layer one after another.

16. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, further comprises forming a first capping layer covering at least the sidewalls of the cell trench and the peripheral trench before forming the first dielectric layer.

17. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 16, wherein the first capping layer is a MTO or a HTO.

18. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, wherein the first dielectric layer is a HDP-CVD oxide.

19. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, wherein etching the first dielectric layer formed on the sidewalls of the cell trench is performed using a wet etching process.

20. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, further comprises forming a second capping layer over the substrate where the photoresist pattern is removed before forming the second dielectric layer.

21. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 20, wherein the second capping layer is a MTO or a HTO.

22. (Original) The method of forming trench isolations for a non-volatile memory device according to claim 13, wherein the second dielectric layer is a HDP-CVD oxide or an USG oxide.